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A Flexible HV Stimulator ASIC with Stimulus-Synchronized Charge Balancing and Embedded CM Regulation for Implantable Peripheral Nerve Stimulation

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Abstract

We present a flexible HV stimulator ASIC for implantable peripheral nerve stimulation applications. Innovative charge balancing techniques are introduced to support diverse stimulation current waveforms, achieving state-of-the-art performance. Fabricated in 130-nm BCD technology, the ASIC has been fully validated through saline characterizations.

Introduction

Implantable peripheral nerve stimulation (PNS) has been developed to treat chronic pain and neurological disorders [1-2]. Recent studies (Fig. 1) emphasize the benefits of spatially selective nerve activation using microelectrodes, which require electrical stimulators to drive multiple electrodes concurrently with specific current waveforms, e.g. sinusoidal signals, to enhance selectivity and therapeutic efficacy [3-7]. In such multipolar PNS systems, each stimulation output unit (SOU) must have an independent current source and sink to minimize crosstalk and sustain high-voltage (HV) signals of >10 V [6, 8]. However, achieving efficient charge balancing (CB) becomes increasingly challenging, particularly in HV implementations.

First, while existing CB approaches demonstrate high precision in addressing SOU mismatches ($I_{MIS,SOU}$), they are primarily developed for biphasic stimulation and often struggle with the increased complexity of sinusoidal waveforms [8-14]. Additionally, these methods frequently introduce excess CB processing time, which can result in unwanted CB artifacts or limit the flexibility of stimulus protocols [14]. Second, unlike simpler mono- or bipolar electrode configurations, multipolar stimulations require additional compensation for mismatches across multiple SOUs ($I_{MIS,CM}$), which is typically managed by creating a low-impedance V_{CM} path [8, 9, 15]. As shown in Fig. 1, high impedance (e.g. a small C_{REF}) can result in substantial offset voltage (ΔV_{CM}) across R_{REF}//C_{REF}, degrading CB precision or even causing CB loop failure [8]. However, such a V_{CM} path often needs power- and area-consuming HV blocks as well as large electrode surfaces to reduce the electrode-tissue impedance (ETI). This reliance on electrode size and geometry can compromise the robustness of PNS implants across different clinical conditions.

To address these challenges, we propose a flexible HV stimulator ASIC (Fig. 2) capable of generating diverse current waveforms to accommodate various therapeutic protocols. To solve mismatch issues, we introduce a stimulus-synchronized CB (SS-CB) technique to address $I_{MIS,SOU}$, and a V_{CM} regulation (CMR) technique to mitigate $I_{MIS,CM}$. Both techniques are versatile enough to support diverse current waveforms.

Architecture and circuit implementation

The ASIC integrates 4 SOUs that can concurrently work as two pairs with different frequencies and amplitudes. An area-efficient SRC+SINK stimulator output architecture (Fig. 3) is adopted and optimized for HV compliance [15]. The digital core can generate flexible waveforms, synthesized by 9-bit IDACs with 1µs time resolution.

Source-sink mismatches within each SOU can cause charge accumulation and offset voltage (V_{OS}) across the corresponding ETI, potentially leading to electrode and tissue damage [10]. Our CB strategy prioritizes minimizing the processing time while maintaining $|V_{OS}|$ at safe levels throughout the stimulus which is optimized to accommodate a 3-σ mismatch range. However, residual V_{OS} will accumulate over a series of stimuli if not periodically corrected. Previous work [15] relies on passive discharging after each stimulus, which can take several milliseconds depending on the ETI. To overcome this, a second detection-correction loop is used during /Φ_{STIM}, quantizing the residual V_{OS} after each stimulus within a short period (~25 µs). Based on the results (D_{CTR}), 3 corrective actions (up, down, or hold) adjust V_{REFA} of the $g_{m,CB}$ amplifier. Consequently, V_M is dynamically modulated during a stimulus train to counteract V_{OS}, following a sigma-delta-like scheme. This SS-CB method can be adapted for typical biphasic stimulation, where V_{OS} often does not rise to unsafe levels within 1 Φ_{STIM}. Thus, only the detection-correction loop is reused during /Φ_{STIM} to dynamically control a 3b-IDAC, counteracting $I_{MIS,SOU}$ in the subsequent stimulus. In both stimulation modes, I_{CB} is always applied simultaneously with the stimulation current I_{STIM}, eliminating excess CB processing time. After a stimulus train, the electrodes can be discharged to the mid-rail V_{CM} via a resistive CM biasing path, further reducing $|V_{OS}|$ levels.

Besides $I_{MIS,SOU}$, imbalances in total source/sink currents can introduce large CB errors, especially with microelectrodes. To address $I_{MIS,CM}$, a CMR method is proposed to operate in conjunction with the SS-CB, which is embedded within the SOUs (Fig. 5). During a stimulus train, CM variations are sensed from all SOU outputs as signal V_{CML}. The AC coupling allows most circuits to work in the low-voltage (LV) domain, achieving precise matching while saving power and area. A current-bleeding $g_{m,CMR}$ amplifier, comparing V_{CML} with a reference V_{CMR}, is optimized for high input impedance and low leakage, making the CMR robust and insensitive to changes in ETI. The resulting I_{OUT} is amplified and distributed to all SOUs as I_{CMR}. A feedback current I_{LOOP} is generated by summing I_{CMR} with I_{CB} at the loop output stage, simultaneously mitigating the $I_{MIS,SOU}$ and $I_{MIS,CM}$. Through this CMR scheme, each SOU contributes to partial V_{CM} regulation in sync with the stimuli, while eliminating the need for additional HV blocks.

Measurement Results

Fig. 6 shows the electrical characterization results with sinusoidal stimulation, demonstrating a significant reduction of $I_{MIS,SOU}$ to <1 nA_{rms} when CB is enabled. Extensive evaluations are further conducted with 4 concurrently working SOUs, including an optional external V_{CM} path for comparison. In both stimulation modes, $|V_{OS}|$ is measured across the entire stimulus train with varying I_E levels and V_{CM} path impedances (Fig. 7 and Fig. 8). When only SS-CB is enabled, $|V_{OS}|$ performance deteriorates as V_{CM} path impedances increase. However, with CMR enabled, $|V_{OS}|$ levels become comparable to those with an ideal low-impedance V_{CM} path (R_{REF}=0), confirming the efficacy of the proposed CMR technique.

Fig. 9 presents saline measurement results using a multi-contact cuff electrode for spatially selective PNS. Without CMR, a fifth electrode contact is connected to an external V_{CM} supply, yet $|V_{OS}|$ performance remains suboptimal due to the relatively high ETI. With CMR enabled, $|V_{OS}|$ performance improves by >50%, consistently maintaining safe levels well below the water oxidation potential [10].

Fig. 10 shows the die photo of this ASIC. A benchmark